Abstract of the Disclosure

A programmable I/O element for an I/O terminal of a logic array is suitable for operating according to high speed I/O modes such as double data rate and zero bus turnaround. The I/O element may include an input block with two registers for registering input signals from the terminal upon alternate clock edges. In addition or alternatively, it may include an output block with two registers that separately register output signals from the array on the same clock edge and a multiplexer that alternately outputs those signals. For bidirectional terminals, the multiplexer output is connectable to the I/O terminal via an output buffer, and an output enable block provides an enable signal to a gating input of the output buffer. Programmable delays may be included in the input, output, and output enable paths, in particular to provide a slower turn-on time than turn-off time for the output buffer.